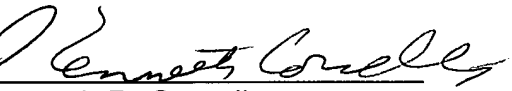
REMARKS

Preliminary to the examination of the above-identified application, please amend claims 2, 6 and 12 and add new claims 26-42. Attached hereto is a marked up version of the changes made to the claims by the current Amendment. The attached page is captioned "Version with Markings to Show Changes Made".

The Examiner is invited to contact the undersigned at (202) 220-4310 to discuss any matter concerning this application. The Office is authorized to charge any fees associated with this Amendment to Kenyon & Kenyon Deposit Account No. 11-0600.

Respectfully submitted,

Date: March 13, 2002



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IN THE CLAIMS:

This amendment amends claims 2, 6, and 12 and adds new claims 26-42 as follows.

2. (Amended) The apparatus of claim 1, wherein other carry generation blocks in the adder circuit are of a size that is a whole number multiple of three stages.

6. (Amended) The apparatus of claim 5, wherein the look-ahead carry adder circuit has carry generate gates and carry propagate gates that are buffered from the critical path to minimize the load on gates in the critical path.

12. (Amended) The method of claim 10, wherein the method further comprises determining an intermediate XOR value for each of said propagate values based on the propagate value and corresponding generate value, wherein sum values are based at least in part on the intermediate XOR values, and wherein intermediate XOR values are determined without using an XOR gate.

26. (New) An apparatus comprising a look-ahead carry adder circuit having a plurality of stages that are grouped into a plurality of carry generation blocks, wherein one of the carry generation blocks is of a size that is a whole number multiple of three stages.

27. (New) The apparatus of claim 26, wherein the look-ahead carry adder circuit has only one critical path.

28. (New) The apparatus of claim 27, wherein the look-ahead carry adder circuit has carry generate gates and carry propagate gates that are buffered from the critical path to minimize the load on gates in the critical path.

29. (New) The apparatus of claim 26, wherein the look-ahead carry adder circuit includes a plurality of tapered transistor stacks.

30. (New) The apparatus of claim 26, wherein the look-ahead carry adder circuit includes at least one gate with a propagate input, a generate input, and only two transistor stacks.

31. (New) The apparatus of claim 26, wherein the look-ahead carry adder circuit contains a NAND tree to generate intermediate XOR values.

32. (New) A method of adding two multi-bit addends, the method comprising:

receiving two multi-bit addends;

determining a propagate value and a corresponding generate value for each bit of the addends;

determining a carry-out value for each propagate value based at least in part on the propagate value and corresponding generate value, wherein the carry-out values are determined by a plurality of carry generation blocks that include a plurality of tapered transistor stacks; and

determining a sum value for each carry-out value based at least on part of the carry-out value.

33. (New) The method of claim 32, wherein the method further comprises determining an intermediate XOR value for each of said propagate values based on the propagate value and corresponding generate value, wherein sum values are based at least in part on the intermediate XOR values, and wherein intermediate XOR values are determined without using an XOR gate.

34. (New) The method of claim 32, wherein there is a single critical path through the plurality of carry generation blocks.

35. (New) The method of claim 34, wherein gates in the critical path have tapered transistor stacks.

36. (New) The method of claim 32, wherein determining one or more of the carry-out values includes combining a propagate value, a generate value, and a carry-in value in a gate that has only two transistor stacks.

37. (New) A look-ahead carry adder circuit, comprising:

inputs to receive two multi-bit addends;

a plurality of blocks each of which is connected to one input bit of both of the multi-bit addends, wherein each block has a propagate output and a generate output;

a plurality of carry generation blocks each having inputs connected to two or more of said propagate outputs and two or more of said generate outputs, wherein each of the carry generation blocks has a plurality of carry outputs, and wherein there is one critical path through the plurality of carry generation blocks; and

a plurality of final blocks each of which is connected to one of said carry outputs and each having a sum output.

38. (New) The look-ahead carry adder circuit of claim 37, wherein the critical path includes an AND-OR-INVERT gate having an output connected to an input of an INVERT-AND-OR gate.

39. (New) The look-ahead carry adder circuit of claim 38, wherein the AND-OR-INVERT gate has only two transistor stacks.

40. (New) The look-ahead carry adder circuit of claim 37, wherein inputs and outputs of gates on the critical path are buffered to reduce the load on the critical path.

41. (New) The look-ahead carry adder circuit of claim 37, wherein the circuit contains a plurality of tapered transistor stacks.

42. (New) The look-ahead carry adder circuit of claim 37, wherein some of the carry generation blocks have a plurality of NAND gates that have a pair of inputs that are connected to one of the propagate outputs and one of the generate outputs through one or more buffers, and wherein each of the NAND gates is connected to an XOR output of a carry generation block through a buffer.